D0 Upgrade Electronics

D0 Workshop 98
July 7, Curia II, 13:30-15:15

Central Tracking Trigger Capabilities

A detailed discussion of the CFT, CPS and FPS triggering capabilities and trigger terms.

Agenda

Overview of the systems.
Description of the CFT/CPS Trigger System
Description of the FPS/CPS Trigger System
Other Systems
Summary

Goal of discussion

We hope with this presentation to inform our collaborators about the planned capabilities for the triggering of the CFT and PS detectors at L1 and what information will be presented to the L2. Therefor we will concentrate on the functionality of the planned hardware and discuss the design of the hardware only when it has a major impact on the functionality.
We need to lock in the functionality for the systems at or within a short time after the workshop.

People

John Anderson	FNAL-DO	PCB Design
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Sudhindra Mani	UC Davis	SIFT
Manuel Martin	FNAL-DO	Broadcaster
Mike Matulik	FNAL-DO	MCM
Jameson Olsen	FNAL-DO	PCB Design
Paul Rubinov	Northwestern	MCM/SIFT
Patrick Sheahan	FNAL-DO	PCB Design
Kin Yip	FNAL-DO	CFT

Documentation locations

Location of latest version of TDR -
Location of WBS Project documentation -

Dzero\Dpfm02\Trigger\WebDocs\Trigger_index.htm

Home page for CFT

http://d0server1.fnal.gov/www/Upg_CFT/cft_home.html

Home page for PS

http://www-d0.fnal.gov/~lucotte/FPS/preliminary.html

Home pages with list of many documents -

http://d0server1.fnal.gov/users/borcherding/Fred_home.html

http://d0server1.fnal.gov/users/Manuel/

Overview

Which detectors have which triggers

	L1	L2	L3
CFT Axial			
	Count	Dig to STTpp & CFTpp	Analog & Digital
	Hit Count		
CFT Stereo			
	--	{Dig to CFTpp}	Analog & Digital
CPS Axial			
	Count	Dig to PSpp	Analog & Digital
CPS Stereo			
	--	Dig to PSpp	Analog & Digital
FPS			
	Count	Dig to PSpp	Analog & Digital

Notes:

Digital to L3 is 'raw' hit data.
Add Analog to L2 for FPS as per review?

CFT/CPS Axial -

L1 - 16 L1 Trigger Terms -
4 Pt Threshold Ranges (Highest, High, Medium, Low) x2 with/without CPS Match,
x2 isolated/non-isolated.

L1 - Sum of CFT Fibers hit - (details not worked out)

L2/L1 Muon - Track List,
1) Highest, lowest Pt per phi bin,
2) for each of 4 Pt threshold bins 6 highest Pt tracks for 24 total.
3) Each tagged with cluster match
But only 6 highest to L1 Muon -no cluster match

L2 PS - Cluster list - tagged with track match

L3 - 'RAW' Digital outputs sent to Virtual SVX for inclusion in L3 DAQ readout. [This is done for all detectors.]

CFT Stereo -

L3 - 'RAW' Digital outputs sent to Virtual SVX for inclusion in L3 DAQ readout.

CPS Stereo -

L2 - digital output to L2pp.

FPS -

L1 - 16 L1 Trigger Terms - for each view U/V number of clusters per quadrant with upstream match/veto.

L2 - Position and width of clusters in U/V with match/veto information

Analog Characteristics

CFT channels

trigger from 3pe which is ~5 fC.
Send into High gain channel - 0 to 50 fC range.

FPS

Divide input into 80:20:2.
Discard 80%
Send 20% into low gain channel
Send 2% into high gain channel.
Forward - Low & High gain to SVX
Forward - High gain V-Out to trigger
Back - Low & High gain to SVX
Back - Low & High gain V-Out to trigger

CPS (Axial & Stereo)

Divide input into 80:20:2.
Discard 80%
Send 20% into low gain channel
Send 2% into high gain channel.
Low & High gain to SVX
Low & High gain V-Out to trigger

Hardware

CFT/CPS Axial channels

- Axial channels to CFT/CPS Trigger FE
- CFT/CPS crates & backplanes
- 96 links to Muon L1
- 80 links to Broadcast crates
- L1 Concentrators - CFT Firmware
- L2 Concentrators for STTpp & CFTpp
  - Passive or active fanout
- L2 Concentrators for PSpp

CFT Stereo channels

- Stereo channels to CFT Stereo FE
- Reduced PS crates and backplanes*
- *75 lnks to Broadcast crates*? ←
- *L2 Concentrators for STTpp & CFTpp*? ←

FPS channels

- All channels to PS Trigger FE
- PS crates and backplanes
- 32 inputs to Broadcast crates
- L1 Concentrators - FPS Firmware
- L2 Concentrators for PSpp

CPS Stereo channels

- All channels to 'reduced' PS Trigger FE
- PS crates and backplanes

FE

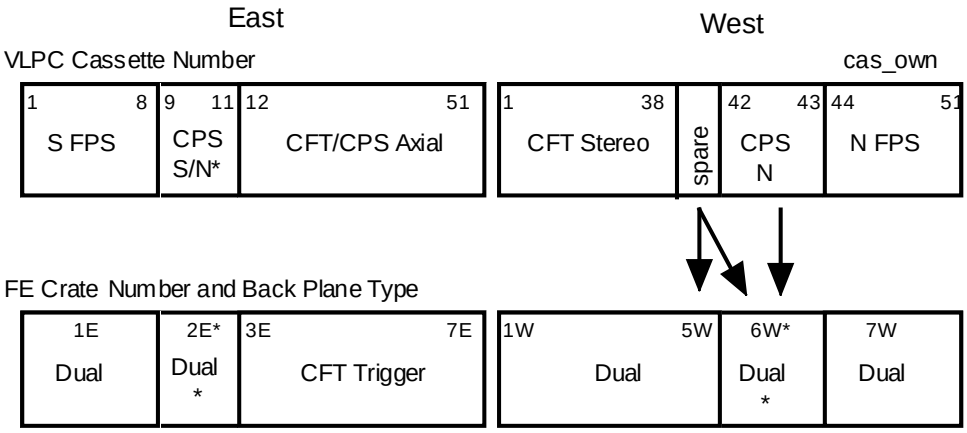
Four types of FE crates & boards.
All share common sub-functionalities.
Design on the function block level and then place function blocks on FE / BP designs.

Broadcaster

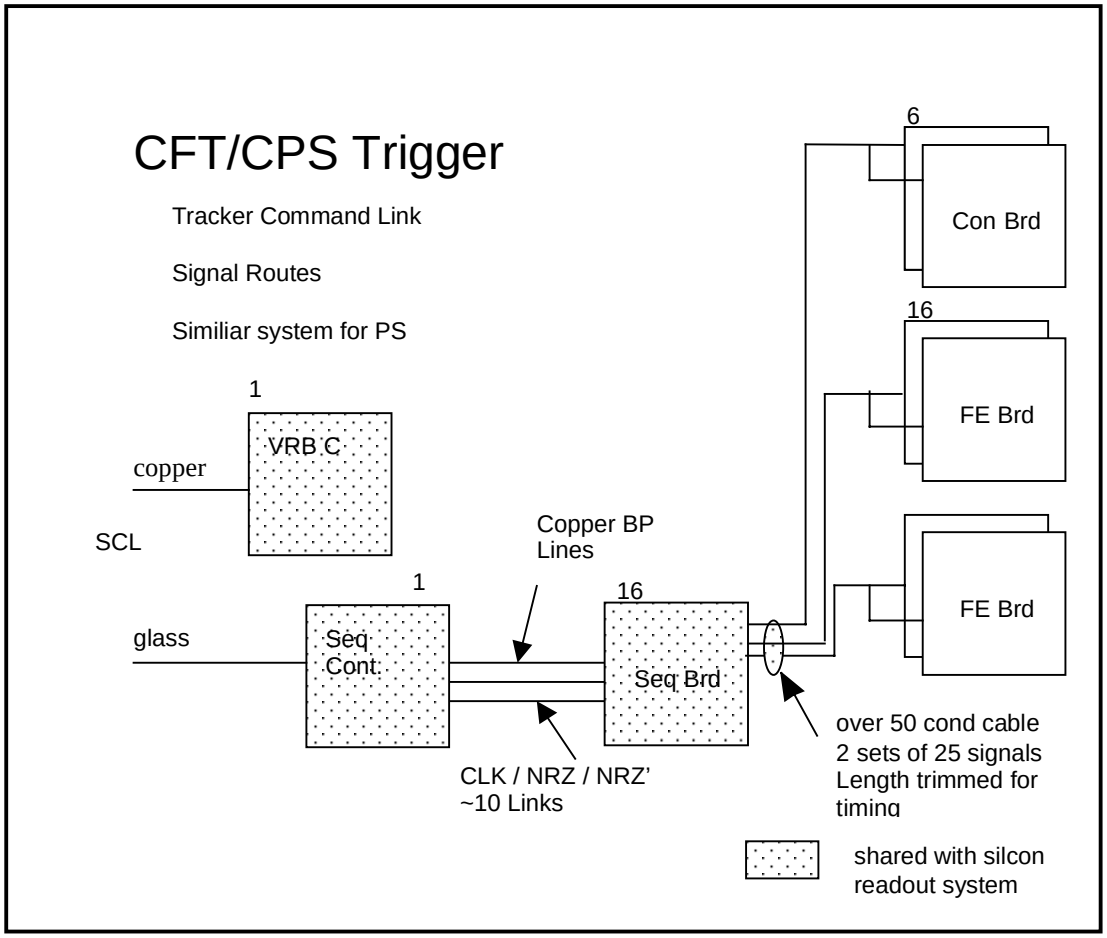
Common hardware.
Separate firmware design and implementation for CFT/CPS and FPS/CPS.

L1 TM

Hardware is Muon Trigger Manager crate and boards.
Separate firmware design and implementation for CFT/CPS and FPS.

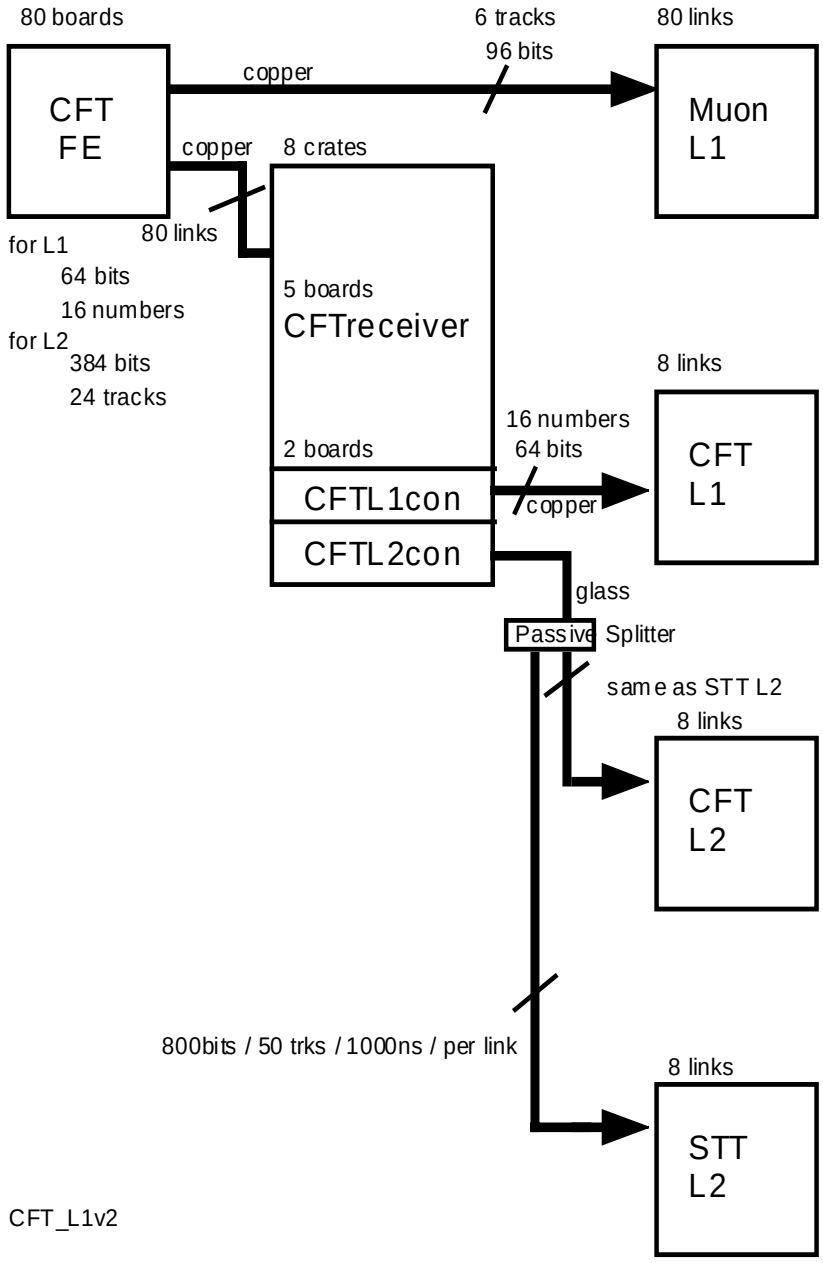


Crate Numbering and Type on the VLPC Cassettes

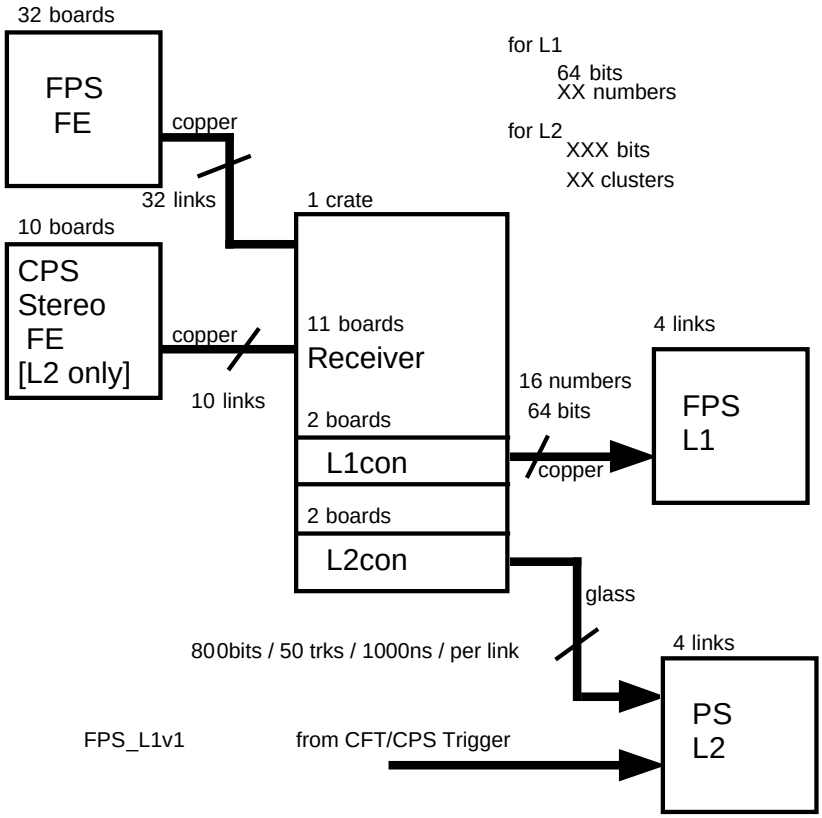


Timing, Control, and L3 Readout for the VLPC Electronics.

Shown is the CFT system - 1 Geographical Sector
FPS system - 1 Geographical Sector
CFT Stereo - 1 Geographical Sector



Schematic of the overall data flow in the CFT L1 and L2 Triggers. The data starts in the CFT FE. One path from there is over 80 serial links to the muon L1. The other path is over another 80 serial links to eight CFT Receiver/ Concentrator Crates. From each crate track counts flow to the CFT L1 crate over one serial link. The track lists flow on another serial link per crate to the L2 preprocessors. A passive splitter at the end of this link fans out the same data to one or more preprocessors.

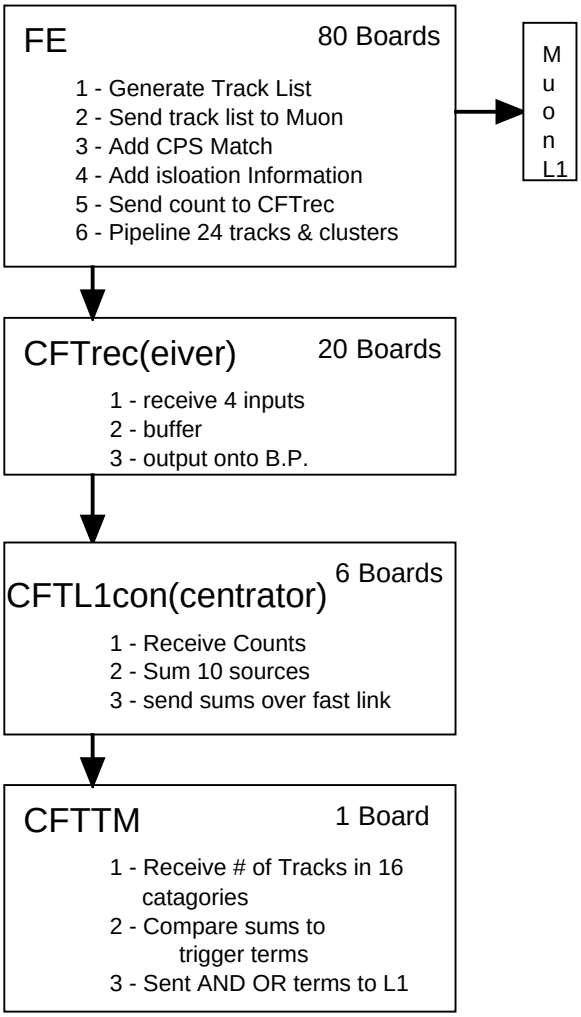


Schematic of the overall data flow in the FPS L1 and L2 Triggers.

Functional Description

Every Crossing (132 ns)

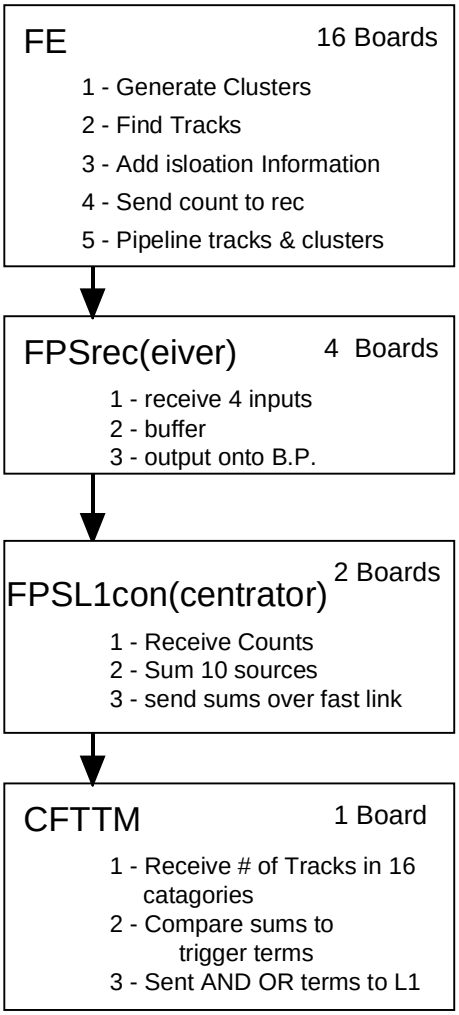
Gen_pic1



Functional description of the FE board for the CFT/CPS during normal operations.

Functional Description

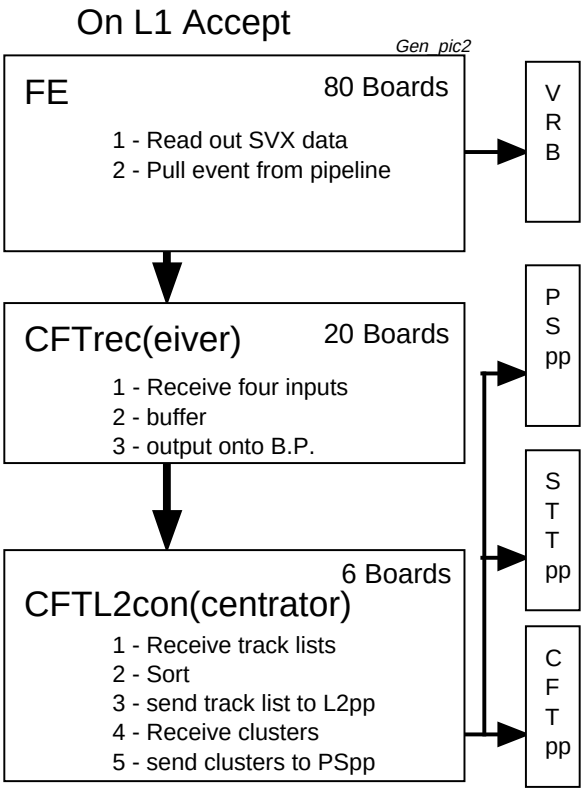
Every Crossing (132 ns)



Functional description of the FE board for the FPS during normal operations.

[NOTE: Details inside boxes is outdated.]

Functional Description

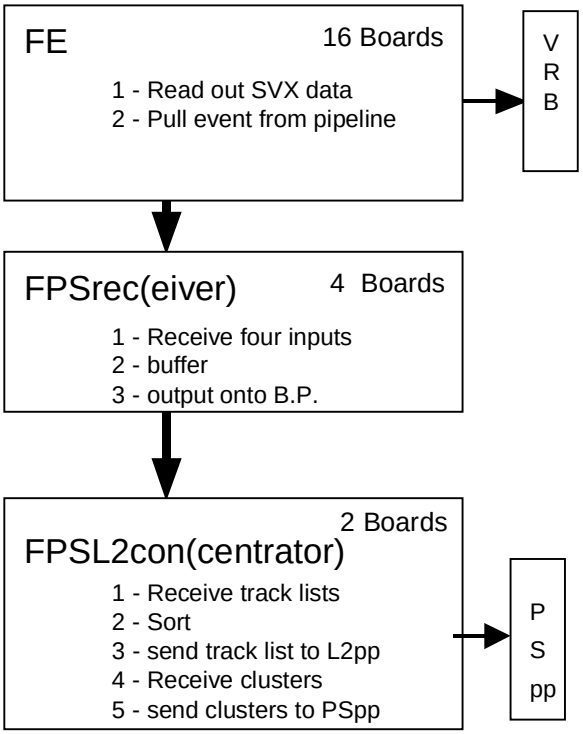


Functional description of the FE board for the CFT/CPS after receiving a L1 Accept.

This operation continues until the data has cleared the entire system, then the system automatically reverts back to normal operation.

Functional Description

On L1 Accept

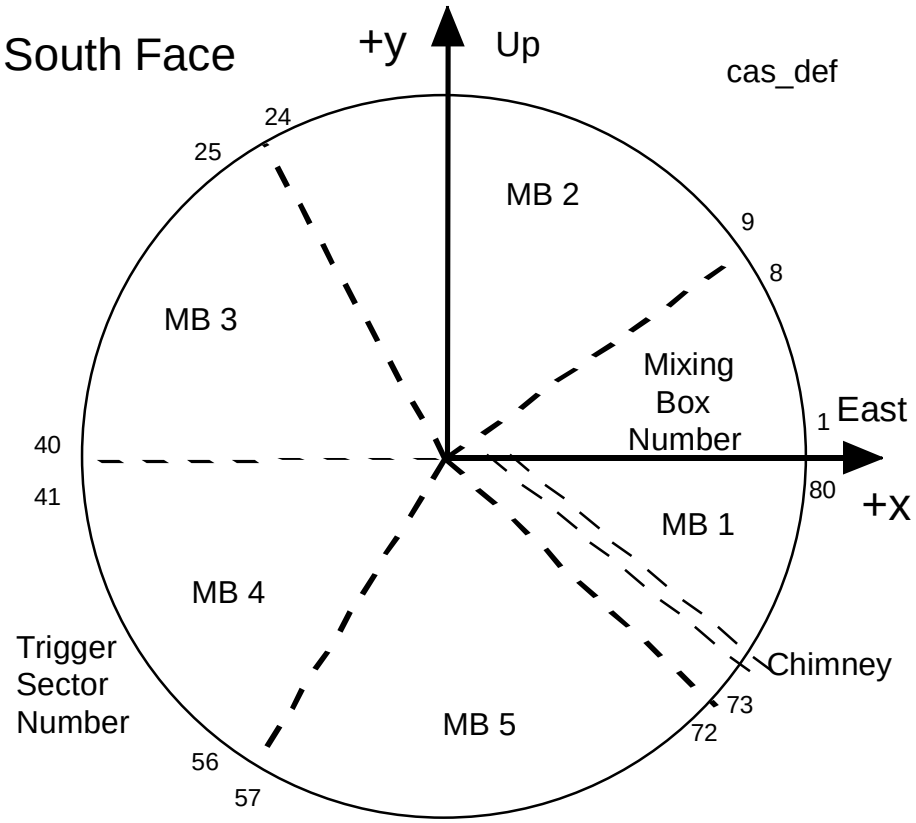


Functional description of the FE board for the FPS after receiving a L1 Accept.

Again this operation continues until the data has cleared the entire system, then the system automatically reverts back to normal operation.

Central Fiber Tracker & Central PreShower, CFT/CPS, Trigger

Location of CFT Trigger Sectors



Description of L1 Trigger

	Offset	Min	Mean	Max	FPLD
HIGHEST	0	18.00	21.40		1 @ 45%
	1	9.00	16.90		
	2	6.50	11.00	21.00	
HIGH	3	4.50	6.80	10.50	1 @ 50%
	4	4.00	5.00	7.00	
MEDIUM	5	3.25	3.90	5.00	2 @ 45%
	6	2.75	3.30	4.00	
	7	2.50	2.80	3.50	
	8	2.20	2.40	2.80	
LOW	9	1.80	2.20	2.50	2 @ 53%
	10	1.80	1.90	2.20	
	11	1.60	1.76	2.00	
	12	1.50	1.62	1.80	
	13	1.40	1.53	1.60	

Pt Threshold binning for the CFT.

This design uses 6 track finding FPLDs on each FE board.

The amount of resources used by an ALTERA 10k series chip for each Pt bin. For Equations & Sort only.

What is the lowest Pt we can trigger on and why?

7 of 8 multiplicity logic requires about 3 times as much logic for the tracking which is about 1/2 of the total -> 3 x 1/2 = 3/2 => 53% above ->> 80%.

A track is ISOLATED if

1 - It is the only track in a sector in any Pt threshold bin.

2 - There are NO tracks in any Pt threshold bins in both neighbors.

Therefor a track is ISOLATED if it is the ONLY track in a fixed 13.5 degree (0.24rad) wedge.

A CPS Cluster Matched track is ISOLATED if

1 - It is the only matched track in a sector in any Pt threshold bin.

2 - There are NO matched tracks in any Pt threshold bins in both neighbors.

[Note it is not necessarily in the center of the wedge.]